Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A power supply circuit comprising:

a DC-DC conversion circuit including a high side transistor and a low side transistor connected in series between a power supply voltage and a reference potential and producing a direct current output voltage as a PWM controlled output[[?]] which is obtained by turning "on" and "off" each of the transistors with each PWM signal; ~~and means~~

a detection circuit for detecting a level of an intermediate node potential at a junction point of the high side transistor and the low side transistor after turning "off" the high side transistor, wherein the detection circuit is directly connected to the high side transistor and the low side transistor at the junction point so as to directly detect the intermediate node potential therefrom; and

means for turning "on" the low side transistor when the intermediate node potential becomes below or equal to a predetermined potential.

2. (Currently amended) A power supply circuit comprising:

a DC-DC conversion circuit including a high side transistor and a low side transistor connected in series between a power supply voltage and a reference potential and producing a direct current output voltage as PWM controlled output which is obtained by turning "on" and "off" each of the transistors with each PWM signal;

means for obtaining an amount of error by comparing the output from the DC-DC conversion circuit to a predetermined reference voltage value;

means for producing a PWM signal of which a pulse width is controlled by the amount of error;

means for supplying the PWM signal to each gate of the transistors in the DC-DC conversion circuit;

a detection circuit for detecting a level of an intermediate node potential at a junction point of the high side transistor and the low side transistor after the high side transistor is turned "off", wherein the detection circuit is directly connected to the high side transistor and the low side transistor at the junction point so as to directly detect the intermediate node potential therefrom; and

means for turning "on" the low side transistor when the intermediate node potential becomes below or equal to a predetermined potential.

3. (Currently amended) The power supply circuit according to claim 1, wherein the ~~means for detecting~~ detection circuit outputs a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to the predetermined potential, which is sufficiently low with respect to the power supply voltage.

4. (Currently amended) The power supply circuit according to claim 1, wherein the ~~means for detecting~~ detection circuit receives the intermediate node potential by a (VDD/2) type logic circuit when setting the power supply voltage to VDD and the reference potential to zero, and outputs a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to a potential below or equal to (VDD/4).

5. (Currently amended) A power supply circuit comprising:

a DC-DC conversion circuit including a high side transistor and a low side transistor connected in series between a power supply voltage and a reference potential and producing a direct current output voltage as PWM controlled output which is obtained by turning "on" and "off" each of the transistors with each PWM signal;

means for obtaining an amount of error by comparing the output from the DC-DC conversion circuit to a predetermined reference voltage value;

means for producing a PWM signal of which a pulse width is controlled by the amount of error; ~~and~~

means for supplying the PWM signal to each gate of the transistors in the DC-DC conversion circuit;

~~means~~ a detection circuit for detecting a level of an intermediate node potential at a junction point of the high side transistor and the low side transistor after the high side transistor is turned "off", wherein the detection circuit is directly connected to the high side transistor and the low side transistor at the junction point so as to directly detect the intermediate node potential therefrom;

PWM signal level detection means for detecting a level of a PWM signal to be supplied to the gate of the low side transistor out of the PWM signals to be supplied to the DC-DC conversion circuit;

means for turning "on" the low side transistor when the ~~first means for detecting~~ detection circuit detects the intermediate node potential lowered below or equal to a predetermined potential; and

means for turning "on" the high side transistor after the PWM signal level detection means ~~second means for detecting~~ detects the level of the PWM signal to be supplied to the gate of the low side transistor lowered below or equal to a predetermined potential.

6. (Currently amended) The power supply circuit according to claim 5, wherein the ~~first means for detecting~~ detection circuit outputs a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to the predetermined potential which is sufficiently low with respect to the power supply voltage, and the PWM signal level detection means ~~second means for detecting~~ outputs a signal for turning "on" the high side transistor when detecting the PWM signal to be supplied to the gate of the low side transistor lowered to the predetermined potential which is sufficiently low with respect to the power supply voltage.

7. (Currently amended) The power supply circuit according to claim 5, wherein the ~~first means for detecting~~ detection circuit receives the intermediate node potential at a (VDD/2) type logic circuit when setting the power supply voltage

to VDD and the reference voltage to zero and outputs a signal for tuning on the low side transistor when detecting the intermediate node potential lowered to a potential below or equal to (VDD/4), and the PWM signal level detection means ~~second means for detecting~~ receives the PWM signal to be supplied to the gate of the low side transistor at a (VDD/2) type logic circuit when setting the power supply voltage to VDD and the reference voltage to zero and outputs a signal for turning "on" the high side transistor after detecting the level of the PWM signal to be supplied to the gate of the low side transistor lowered to a potential below or equal to (VDD/4).

8. (Currently amended) The power supply circuit according to claim 2, ~~further comprising a~~ wherein the detection circuit ~~which~~ outputs a detection signal indicating that the intermediate node potential has exceeded the reference potential after returning from an undershoot at a level lower than the reference potential when the low side transistor is turned on during an "off"-period of the high side transistor, wherein means for producing further includes a function of turning "off" the low side transistor being in an on-state by controlling, based on a detection signal of the detection circuit, a pulse width of the PWM signal to be supplied to the gate of the low side transistor out of the PWM signals to be supplied to the DC-DC conversion circuit.

9. (Original) The power supply circuit according to claim 1, further comprising an error amplifier that produces an error signal by comparing the output voltage of the DC-DC conversion circuit with a reference voltage value of a reference voltage supply.

10. (Original) The power supply circuit according to claim 1, further comprising an output driver for receiving an input of the PWM signal.

11. (Original) The power supply circuit according to claim 1, further comprising a rectifier coil and a stabilizing capacitance connected in series between an intermediate node.

12. (Original) The power supply circuit according to claim 1, further comprising a diode connected between the source and drain of the low side transistor.

13. (Original) The power supply circuit according to claim 1, wherein the output driver forms gate pulses to be supplied to the high side transistor and the low side transistor.

14. (Original) The power supply circuit according to claim 1, wherein the high side transistor and the low side transistor have a drain in common.

15. (Original): A power supply circuit comprising:

a DC-DC conversion circuit including a high side transistor and a low side transistor connected in series between a power supply voltage and a reference potential and producing a voltage as PWM controlled output which is obtained by turning "on" and "off" each of the transistors with each PWM signal; and

a ~~PWM circuit and output driver~~ detection circuit that detects a level of an intermediate node potential at a junction point of the high side transistor and the low side transistor after turning "off" the high side transistor wherein the detection circuit is directly connected to the high side transistor and the low side transistor at the junction point so as to directly detect the intermediate node potential therefrom, and ~~turning~~ a PWM circuit and output driver that turns "on" the low side transistor when the intermediate node potential becomes below or equal to a predetermined potential.

16. (Original) The power supply circuit according to claim 15, wherein the PWM circuit and the output driver output a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to the predetermined potential which is sufficiently low with respect to the power supply voltage.

17. (Original) The power supply circuit according to claim 15, wherein the PWM circuit and output driver receive the intermediate node potential by a (VDD/2) type logic circuit when setting the power supply voltage to VDD and the

reference potential to zero, and output a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to a potential below or equal to (VDD/4).

18. (Currently amended) The power supply circuit according to claim 2, wherein the ~~means for detecting~~ detection circuit outputs a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to the predetermined potential, which is sufficiently low with respect to the power supply voltage.

19. (Currently amended) The power supply circuit according to claim 2, wherein the ~~means for detecting~~ detection circuit receives the intermediate node potential by a (VDD/2) type logic circuit when setting the power supply voltage to VDD and the reference potential to zero, and outputs a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to a potential below or equal to (VDD/4).

20. (Currently amended) The power supply circuit according to claim 5, ~~further comprising a~~ wherein the detection circuit ~~which~~ outputs a detection signal indicating that the intermediate node potential has exceeded the reference potential after returning from an undershoot at a level lower than the reference potential when the low side transistor is turned "on" during an "off" period of the high side transistor, wherein the means for producing further includes a function of turning "off' the low side transistor being in an on-state by controlling, based on a detection signal of the detection circuit, a pulse width of the PWM signal to be supplied to the gate of the low side transistor out of the PWM signals to be supplied to the DC-DC conversion circuit.